

CLAIMS

What is claimed is:

1 1. A signal processor for performing dyadic digital signal
2 processing instructions having main operations and sub
3 operations, the signal processor comprising:

4 at least one signal processing unit including,

5 a first multiplier and a first adder to execute a
6 main operation of a dyadic digital signal processing
7 instruction,

8 a second multiplier and a second adder to execute
9 a sub operation of the dyadic digital signal
10 processing instruction,

11 each of the first and second adders and the first
12 and second multipliers having a multiplexer at its
13 input to configure the signal processing unit to
14 execute the main operation and the sub operation of
15 the dyadic digital signal processing instruction, and

16 an accumulator having registers to couple to the
17 first multiplier or the first adder to provide
18 operands or store intermediate results therefrom and
19 to couple to the second multiplier or the second adder

20 to provide an operand for the sub operation of the
21 dyadic digital signal processing instruction and to
22 store results of the sub operation, the accumulator
23 register having a register to couple to the buffer
24 memory to store the digital signal processed output
25 generated by the dyadic digital signal processing
26 instruction.

1 2. The signal processor of claim 1 for performing dyadic
2 digital signal processing instructions, the signal processor
3 further comprising:

4 a reduced instruction set computer (RISC) control unit and
5 a pipeline controller to predecode the dyadic digital signal
6 processing instruction into a plurality of preliminary
7 instruction execution signals, and

8 wherein the at least one signal processing unit further
9 includes

10 a plurality of final decoders coupled to a
11 plurality of multiplexers, each of the first and
12 second adders and first and second multipliers having
13 an input multiplexer from the plurality of
14 multiplexers to receive operands responsive to the
15 selection by those of the plurality of final decoders

16 coupled thereto.

1 3. The signal processor of claim 1 for performing dyadic
2 digital signal processing instructions, wherein,
3 the main operation of the dyadic digital signal processing
4 instruction is one of the set of multiplication, addition,
5 comparison with a minimum or maximum value, and no operation.

1 4. The signal processor of claim 3 for performing dyadic
2 digital signal processing instructions, wherein,
3 the sub operation of the dyadic digital signal processing
4 instruction is one of the set of multiplication, addition,
5 comparison with a minimum or maximum value, and no operation
6 which differs from the main operation.

1 5. The signal processor of claim 1 for performing dyadic
2 digital signal processing instructions, wherein,
3 the main operation of the dyadic digital signal processing
4 instruction is selected to be one of the set of multiplication,
5 addition, comparison with a minimum or maximum value, and no
6 operation and the sub operation of the dyadic digital signal
7 processing instruction is selected to be a no operation.

1 6. The signal processor of claim 2 for performing dyadic
2 digital signal processing instructions, wherein,
3 the RISC control unit includes three adders, a memory
4 address generator, a multiplier, and a barrel shifter to
5 predecode the dyadic digital signal processing instruction into
6 the plurality of preliminary instruction execution signals.

1 7. The signal processor of claim 1 for performing dyadic
2 digital signal processing instructions, the signal processor
3 further comprising:

4 a data memory coupled to the RISC control unit and the at
5 least one signal processing unit for storing operands and
6 results of the execution of the dyadic digital signal processing
7 instruction, and

8 a program memory coupled to the pipeline control, the
9 program memory to store dyadic digital signal processing
10 instructions for execution by the at least one digital signal
11 processing unit.

1 8. The signal processor of claim 1 for performing dyadic
2 digital signal processing instructions, the signal processor
3 further comprising:

4 a host interface to interface to an external host computer,
5 an external memory interface to read and write data to an
6 external memory,
7 clock and phase-locked loop to control the timing of
8 operations of the application specific signal processor,
9 a memory movement engine coupled to the buffer memory to
10 transceive data thereto and therefrom, and
11 wherein the at least one signal processing unit further
12 includes,
13 a data typer and aligner to order the bits of the operands
14 for execution with the main operation, a third adder to add
15 operands together and a compressor to compress more than two
16 operands into a pair of operands.

1 9. A method of performing dyadic digital signal processing
2 (DSP) instructions, the method comprising:
3 fetching a dyadic DSP instruction having a main operation
4 and a sub operation;
5 predecoding the dyadic DSP instruction to generate
6 predecoded instruction signals; and
7 decoding the predecoded instruction signals to generate
8 select signals to select the inputs of multiplexers of DSP
9 functional blocks to execute the main operation and the sub

10 operation.

1 10. The method of claim 9 of performing dyadic digital
2 signal processing (DSP) instructions, wherein,
3 the main operation and the sub operation are performed in
4 parallel during the same cycle.

1 11. The method of claim 9 of performing dyadic digital
2 signal processing (DSP) instructions, wherein,
3 the main operation and the sub operation are performed
4 sequentially during different cycles.

1 12. The method of claim 9 of performing dyadic digital
2 signal processing (DSP) instructions, wherein,
3 the main operation and the sub operation are two different
4 operations selected from the set of multiplication, addition,
5 comparison with a minimum or maximum value, and no operation.

1 13. The method of claim 9 of performing dyadic digital
2 signal processing (DSP) instructions, wherein,
3 the DSP functional blocks include a first and second adder
4 and a first and second multiplier, the DSP functional blocks to
5 perform addition, subtraction and a comparison with a minimal

6 value or a maximum value.

1 14. An instruction set architecture (ISA) for execution of
2 operations within a digital signal processor, the instruction
3 set architecture comprising:

4 a set of instructions for operation within a digital
5 signal processor wherein each instruction includes a
6 first operand accessed directly from memory, a second
7 operand accessed directly from memory of a local
8 register, and a destination register to store results,
9 the set of instructions including,

10 a 20-bit DSP instruction, and

11 a 40-bit DSP instruction,

12 the set of instructions to accelerate
13 calculations within the digital signal processor of
14 the type where $D = [(A \text{ operation one } B) \text{ operation two } C]$ where operation one and operation two are separate
15 signal processing operations.
16

1 15. The instruction set architecture (ISA) of claim 14 for
2 execution of operations within a digital signal processor,
3 wherein,

4 the twenty bit instruction uses mode bits in

5 control registers (i.e. mode registers) and the forty
6 bit instruction has a control extension to override
7 mode registers.

1 16. The instruction set architecture (ISA) of claim 14 for
2 execution of operations within a digital signal processor,
3 wherein,
4 the set of instructions further includes a dyadic instruction
5 to execute two operations in one instruction .

1 17. The instruction set architecture (ISA) of claim 16 for
2 execution of operations within a digital signal processor,
3 wherein
4 the two operations of the dyadic instruction for
5 execution in one instruction are DSP operations.

1 18. The instruction set architecture (ISA) of claim 17 for
2 execution of operations within a digital signal processor,
3 wherein
4 the DSP operations are of the set of operations of
5 multiplication, addition, extremum, and no operation.

1 19. A dyadic digital signal processing (DSP) instruction

2 for execution in digital signal processor, the dyadic DSP
3 instruction comprising:
4 a main DSP operation and a sub DSP operation to be executed
5 in one processor cycle;
6 a first field indicating execution of the main DSP
7 operation and the sub DSP operation to be executed in sequence
8 serially or executed substantially simultaneously in parallel;
9 and
10 a second field indicating a first operand, a third field
11 indicating a second operand, and a fourth field indicating a
12 destination.

1 20. The dyadic digital signal processing (DSP) instruction
2 of claim 19 for execution in a digital signal processor, wherein
3 the DSP operations are of the set of operations of
4 multiplication, addition, extremum, and no operation.